

# Course Syllabus

## FPGA Prototyping

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### **Objective:**

The goal of the course is to study the basic principles and methods of FPGA prototyping. The course also focuses on the study of principles of IC prototyping; hardware and software; design strategies and methods.

### **Class Hours:**

The course duration is 20 hours, lectures volume is 10 hours and laboratory works are 10 hours.

### **Reference Materials:**

To study the course the necessary list of references is given below.

1. D. Amos, Au. Lesea, R. Richter. "FPGA-Based Prototyping Methodology Manual", 2011
2. D. Vega. FPGA 133 Success Secrets - 133 Most Asked Questions on FPGA - What You Need to Know. Emereo Publishing, 2014
3. V. Sklyarov, L. Skliarova, A. Barkalov, L. Titarenko. Synthesis and Optimization of FPGA-Based Systems. Springer; 2014
4. P. Chu Pong, "FPGA Prototyping By Verilog Examples", Xilinx Spartan, 3rd version, 2008
5. High-performance ASIC Prototyping Systems (HAPS) Datasheets
6. Spartan-3A/3AN FPGA Starter Kit Board User Guide, 2010

### **Lectures (10 hours):**

#### **Topic 1.1 (2 hours) – Introduction**

- Different kinds of programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA manufacturers (Xilinx, Altera, Actel, Lattice Semiconductor, Atmel). FPGA applications. Adjoining devices. Instruments and software.

#### **Topic 1.2 (2 hours) –The Structure of FPGA**

- FPGA general description. Different kinds of FPGA packages. FPGA architecture. Internal hard modules of FPGA (CLB, Block RAM, DCM), their meanings and usage. Different kinds of I/O modules, their usage and configuration.

#### **Topic 1.3 (2 hours) – FPGA Design Flow**

- Architecture design. Project design using Verilog Hardware Description Language (HDL). Defining testing methodology and testbench design. RTL simulation, synthesizing, implementation, gate level simulation of design. Reusing of internal hard modules during design and implementation.

#### **Topic 1.4 (2 hours) – Testing Methodology**

- Functional and gate level testing. SDF file description and usage.

#### **Topic 1.5 (2 hours) – FPGA Configuration**

Different types of FPGA configuration files. Generation of configuration file and its loading into FPGA.

### **Laboratory Works (10 hours):**

Topic 2.1 (5 hours) – Modeling of Rotary Encoder Controlled Multi-LED Dimmer

Topic 2.2 (5 hours) – Modeling of SVGA Display Controller